Standards Manager Web Standards List

VITA-VMEbus International Trade Association

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1	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2024	VITA	0
2	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2024	VITA	0
3	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2024	VITA	
4	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2024	VITA	
5	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2024	VITA	
6	46.10	Rear Transition Module for VPX	2024	VITA	
7	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2024	VITA	
8	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2024	VITA	
9	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2024	VITA	
10	87.0	High Density (HD) MT Circular Connector - Type 1	2024	VITA	0
11	91.0	Connector for Higher Density VPX Applications	2024	VITA	0
12	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2024	VITA	
13	68.3	Reference SI Model Standard for Gen4 and Higher Speeds	2024	VITA	
14	42.0 ERTA	XMC	2023	VITA	
15	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2023	VITA	0
16	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2023	VITA	0
17	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By Cooling Technology	2023	VITA	0
18	62.1	Three Phase High-Voltage Power Supply Front- End in a 3U Plug-In Module Standard	2023	VITA	0
19	65.0	OpenVPX System Standard	2023	VITA	0
20	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2023	VITA	0
21	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2023	VITA	0
22	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2022	VITA	0
23	66.5 ERTA	Optical Interconnect on VPX - Hybrid Variants	2022	VITA	
24	46.11	System Management on VPX	2022	VITA	293
25	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2022	VITA	20
26	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2022	VITA	60

27	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2022	VITA	59
28	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2022	VITA	54
29	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2022	VITA	36
30	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2022	VITA	102
31	66.5	Optical Interconnect on VPX - Hybrid Variants	2022	VITA	84
32	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2022	VITA	77
33	74.0	Compliant System Small Form Factor Module Base Standard	2022	VITA	91
34	78.00	SpaceVPX Systems	2022	VITA	624
35	88.0	Switched Mezzanine Card Plus (XMC+) Standard	2021	VITA	44
36	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2021	VITA	60
37	42.0	XMC	2021	VITA	83
38	65.0	OpenVPX System Standard	2021	VITA	921
39	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2021	VITA	80
40	68.2	VPX Standard S-Parameter Definition	2021	VITA	28
41	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2020	VITA	28
42	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2020	VITA	28
43	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2020	VITA	70
44	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2020	VITA	70
45	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	47
46	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	38
47	46.30	Higher Data Rate VPX	2020	VITA	30
48	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	16
49	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	47
50	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	54
51	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	40
52	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	47
53	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	38
54	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	40

55	46.30	Higher Data Rate VPX	2020	VITA	30
56	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	16
57	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	47
58	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	54
59	46.31	Higher Data Rate VPX, Solder Tail	2020	VITA	30
60	46.31	Higher Data Rate VPX, Solder Tail	2020	VITA	31
61	65.0	OpenVPX System Standard	2019	VITA	868
62	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	26
63	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	35
64	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	18
65	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	19
66	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	121
67	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	122
68	65.0	OpenVPX System Standard	2019	VITA	868
69	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	80
70	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	64
71	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	26
72	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	25
73	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	22
74	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	26
75	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	35
76	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	18
77	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	19
78	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	122
79	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	13
80	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	81
81	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	26

82	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	27
83	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	22
84	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant â__The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	15
85	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant â__The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	16
86	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	67
87	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	28
88	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	34
89	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2018	VITA	45
90	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	31
91	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	47
92	46.4	PCI Expressì_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Expressì_ Fabric in the VITA46 environment and to define the mapping of the PCI Expressì Links on the VPX connector.	2018	VITA	21
93	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	32
94	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	27
95	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	92
96	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	58
97	41.1	VXS 4X InfiniBandâ__ Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	24
98	41.2	VXS 4X Serial RapidIOâ__ Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	25
99	42.1	XMC Switched Mezzanine Card: Parallel RapidIOâ__ 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	30
100	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	15
101	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	53
102	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	54
103	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	19
104	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	15

105	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	16
106	57.4 ERTA	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	73
107	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	67
108	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	30
109	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	15
110	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	33
111	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	47
112	46.4	PCI Express on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express Fabric in the VITA46 environment and to define the mapping of the PCI Express Links on the VPX connector.	2018	VITA	21
113	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	32
114	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	27
115	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	92
116	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	53
117	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	28
118	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	34
119	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	60
120	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	26
121	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	25
122	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	54
123	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	19
124	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	50
125	49.02	VITA Radio Transport (VRT) Standard for Electromagnetic Spectrum: Signals and Applications	2017	VITA	361
126	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	359
127	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	33

128	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	24
129	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0]. PDF Version.	2017	VITA	58
130	65.0	OpenVPX System Standard	2017	VITA	769
131	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	46
132	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2017	VITA	41
133	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	25
134	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	49
135	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	92
136	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	32
137	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	359
138	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	50
139	53.0	Standard for Commercial Technology Market Surveillance â__ This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	24
140	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	24
141	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	51
142	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	92
143	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	19
144	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	22
145	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2016	VITA	97
146	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	46
147	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	21
148	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	36
149	42.0	XMC	2016	VITA	44
150	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2016	VITA	47
151	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2016	VITA	26
152	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2016	VITA	61
153	78.00 ERTA	SpaceVPX Systems	2016	VITA	410
154	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	22
155	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	19

156	67.1 ERTA	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2016	VITA	24
157	62	Modular Power Supply Standard	2016	VITA	97
158	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2016	VITA	45
159	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	46
160	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	21
161	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	36
162	42.0	XMC	2016	VITA	44
163	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	17
164	49A	Spectrum Survey Interoperability Specification	2015	VITA	44
165	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	184
166	46.10	Rear Transition Module for VPX	2015	VITA	38
167	46.11	System Management on VPX	2015	VITA	228
168	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	42
169	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	43
170	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	18
171	78.00	SpaceVPX Systems	2015	VITA	404
172	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines â__Serial FPDPâ__, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	42
173	46.10	Rear Transition Module for VPX	2015	VITA	38
174	46.11	System Management on VPX	2015	VITA	228
175	49A	Spectrum Survey Interoperability Specification	2015	VITA	44
176	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	184
177	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	18
178	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	17
179	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	43
180	78.00	SpaceVPX Systems	2015	VITA	410
181	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	25
182	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	27
183	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	11

184	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By__Cooling Technology	2014	VITA	37
185	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	34
186	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	17
187	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (__PCI Mezzanine Card__) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	15
188	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	11
189	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	48
190	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	25
191	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	27
192	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	35
193	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	17
194	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (__PCI Mezzanine Card__) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	15
195	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	11
196	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	48
197	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	11
198	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By__Cooling Technology	2014	VITA	37
199	42.0	XMC	2014	VITA	40
200	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2014	VITA	37
201	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2013	VITA	109
202	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2013	VITA	33
203	46.9 ERTA	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2013	VITA	71
204	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2013	VITA	32
205	46.11	System Management on VPX	2013	VITA	208
206	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2013	VITA	34
207	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	18
208	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	27
209	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2013	VITA	15

210	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	54
211	74.0	Compliant System Small Form Factor Module Base Standard	2013	VITA	67
212	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	16
213	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	27
214	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	54
215	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	23
216	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	142
217	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	26
218	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	20
219	66.1	Optical Interconnect On VPX - MT Variant â__The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	14
220	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	42
221	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	22
222	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	141
223	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	25
224	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	19
225	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	60
226	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2012	VITA	555
227	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2012	VITA	23
228	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2012	VITA	24
229	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2012	VITA	25
230	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	16
231	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2012	VITA	45
232	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2012	VITA	91
233	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	44

234	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	62
235	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2012	VITA	28
236	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2012	VITA	47
237	46.4	PCI Express on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express Fabric in the VITA46 environment and to define the mapping of the PCI Express Links on the VPX connector.	2012	VITA	21
238	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2012	VITA	27
239	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2012	VITA	17
240	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2012	VITA	32
241	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	52
242	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2011	VITA	57
243	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	55
244	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	15
245	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	97
246	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	72
247	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	33
248	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	29
249	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	305
250	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	66
251	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	100
252	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2011	VITA	48
253	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	18
254	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	37
255	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2011	VITA	27
256	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2011	VITA	21
257	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	46
258	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	123
259	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	52

260	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2011	VITA	19
261	66.1	Optical Interconnect On VPX - MT Variant The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2011	VITA	14
262	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	46
263	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	27
264	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	64
265	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	95
266	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	13
267	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	72
268	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	53
269	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	31
270	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	16
271	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	123
272	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	52
273	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	35
274	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	303
275	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	100
276	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	2011	VITA	48
277	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	51
278	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2010	VITA	555
279	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2010	VITA	82
280	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2010	VITA	24
281	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2010	VITA	21
282	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2010	VITA	17
283	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2010	VITA	33
284	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2010	VITA	53
285	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2010	VITA	48

286	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2010	VITA	70
287	46.4	PCI Express_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express_ Fabric in the VITA46 environment and to define the mapping of the PCI Express_ Links on the VPX connector.	2010	VITA	17
288	46.10	Rear Transition Module for VPX	2009	VITA	38
289	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2009	VITA	19
290	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	17
291	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	18
292	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	179
293	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	184
294	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2009	VITA	35
295	41.6	VXS 1X Gigabit Ethernet Control Channel Layer Standard	2009	VITA	32
296	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2009	VITA	18
297	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2009	VITA	43
298	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2009	VITA	27
299	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2008	VITA	79
300	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2008	VITA	37
301	42.0	XMC	2008	VITA	40
302	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2008	VITA	21
303	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	109
304	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	107
305	47	This standard defines environmental, design and construction, safety, and quality requirements for commercial-off-the-shelf (COTS) plug-in units (cards, modules, etc.) intended for mobile applications.	2007	VITA	22
306	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2006	VITA	26
307	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2006	VITA	60
308	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	2006	VITA	14
309	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	2006	VITA	64
310	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	2006	VITA	18
311	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	2006	VITA	135

312	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2006	VITA	66
313	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2003	VITA	40
314	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2003	VITA	42
315	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2003	VITA	48
316	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2003	VITA	100
317	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2002	VITA	37
318	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2001	VITA	68
319	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second. Reaffirmed in 2009. Stabilized in 2014.	1999	VITA	51
320	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	1999	VITA	74
321	1.4	VME64x Live Insertion System Requirements	1998	VITA	29
322	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	1998	VITA	54
323	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	1998	VITA	125
324	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	1998	VITA	48
325	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	1998	VITA	66
326	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	1998	VITA	20
327	19.0	Summary and Introduction to the BusNet Standard	1997	VITA	19
328	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	1997	VITA	137
329	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	1997	VITA	98
330	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	1997	VITA	50
331	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	1996	VITA	15
332	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	1996	VITA	39
333	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	1996	VITA	63
334	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	1995	VITA	43
335	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	1995	VITA	16
336	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	1995	VITA	97
337	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	1995	VITA	66

338	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	1994	VITA	305
339	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	1994	VITA	55