Standards Manager Web Standards List

VITA-VMEbus International Trade Association

Id	Number	Title	Year	Organization	Page
1	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	
2	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	
3	46.30	Higher Data Rate VPX	2020	VITA	
4	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	
5	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	
6	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	
7	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	
8	65.0	OpenVPX System Standard	2019	VITA	
9	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	
10	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	
11	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	
12	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	
13	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	
14	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	
15	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	
16	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	
17	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	
18	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	
19	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	
20	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	
21	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	
22	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	
23	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	
24	46.4	PCI Express on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express Fabric in the VITA46 environment and to define the mapping of the PCI Express Links on the VPX connector.	2018	VITA	

25	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	
26	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	
27	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	
28	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	
29	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	
30	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	
31	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	
32	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	
33	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	
34	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	
35	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	
36	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	
37	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	
38	57.4 ERTA	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	
39	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	
40	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	
41	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0]. PDF Version.	2017	VITA	
42	65.0	OpenVPX System Standard	2017	VITA	
43	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	
44	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2017	VITA	
45	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	
46	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	
47	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	
48	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	
49	49.02	VITA Radio Transport (VRT) Standard for Electromagnetic Spectrum: Signals and Applications	2017	VITA	

50	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	
51	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	
52	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	
53	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	
54	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	
55	42.0	XMC	2016	VITA	
56	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2016	VITA	
57	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2016	VITA	
58	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2016	VITA	
59	78.00 ERTA	SpaceVPX Systems	2016	VITA	
60	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	
61	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	
62	67.1 ERTA	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2016	VITA	
63	62	Modular Power Supply Standard	2016	VITA	
64	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2016	VITA	
65	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	
66	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	
67	78.00	SpaceVPX Systems	2015	VITA	
68	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	
69	49A	Spectrum Survey Interoperability Specification	2015	VITA	
70	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	
71	46.10	Rear Transition Module for VPX	2015	VITA	
72	46.11	System Management on VPX	2015	VITA	
73	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	
74	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	
75	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	

76	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (__PCI Mezzanine Card__) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	
77	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	
78	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	
79	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	
80	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By__ Cooling Technology	2014	VITA	
81	42.0	XMC	2014	VITA	
82	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2014	VITA	
83	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	
84	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	
85	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	
86	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2013	VITA	
87	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	
88	74.0	Compliant System Small Form Factor Module Base Standard	2013	VITA	
89	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2013	VITA	
90	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2013	VITA	
91	46.9 ERTA	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2013	VITA	
92	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2013	VITA	
93	46.11	System Management on VPX	2013	VITA	
94	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2013	VITA	
95	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	
96	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	
97	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	
98	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2012	VITA	
99	46.3	Serial RapidIO__ on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2012	VITA	
100	46.4	PCI Express¦_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express¦_ Fabric in the VITA46 environment and to define the mapping of the PCI Express¦_ Links on the VPX connector.	2012	VITA	
101	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2012	VITA	

102	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2012	VITA	
103	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2012	VITA	
104	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	
105	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	
106	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	
107	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	
108	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2012	VITA	
109	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2012	VITA	
110	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2012	VITA	
111	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2012	VITA	
112	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	
113	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2012	VITA	
114	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2012	VITA	
115	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2011	VITA	
116	66.1	Optical Interconnect On VPX - MT Variant The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2011	VITA	
117	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	
118	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2011	VITA	
119	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	
120	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	
121	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	
122	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	
123	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	
124	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	
125	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	

126	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	
127	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	
128	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2011	VITA	
129	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	
130	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	
131	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2011	VITA	
132	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2011	VITA	
133	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	
134	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	
135	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	
136	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2010	VITA	
137	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2010	VITA	
138	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2010	VITA	
139	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2010	VITA	
140	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2010	VITA	
141	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2010	VITA	
142	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2010	VITA	
143	46.4	PCI Express® on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express® Fabric in the VITA46 environment and to define the mapping of the PCI Express® Links on the VPX connector.	2010	VITA	
144	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2010	VITA	
145	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2010	VITA	
146	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2009	VITA	
147	46.10	Rear Transition Module for VPX	2009	VITA	
148	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2009	VITA	
149	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	
150	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	

151	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	
152	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	
153	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2009	VITA	
154	41.6	VXS 1X Gigabit Ethernet Control Channel Layer Standard	2009	VITA	
155	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2009	VITA	
156	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2009	VITA	
157	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2008	VITA	
158	42.0	XMC	2008	VITA	
159	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2008	VITA	
160	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2008	VITA	
161	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	
162	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	
163	47	This standard defines environmental, design and construction, safety, and quality requirements for commercial-off-the-shelf (COTS) plug-in units (cards, modules, etc.) intended for mobile applications.	2007	VITA	
164	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2006	VITA	
165	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2006	VITA	
166	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2003	VITA	
167	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2003	VITA	
168	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2003	VITA	
169	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2003	VITA	
170	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2002	VITA	
171	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2001	VITA	
172	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second. Reaffirmed in 2009. Stabilized in 2014.	1999	VITA	
173	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	1999	VITA	
174	1.4	VME64x Live Insertion System Requirements	1998	VITA	
175	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	1998	VITA	
176	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	1998	VITA	

177	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	1998	VITA	
178	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	1998	VITA	
179	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	1998	VITA	
180	19.0	Summary and Introduction to the BusNet Standard	1997	VITA	
181	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	1997	VITA	
182	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	1997	VITA	
183	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	1997	VITA	
184	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	1996	VITA	
185	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	1996	VITA	
186	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	1996	VITA	
187	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	1995	VITA	
188	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	1995	VITA	
189	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	1995	VITA	
190	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	1995	VITA	
191	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	1994	VITA	
192	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	1994	VITA	